Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A field programmable device (FPD) implementing a circuit logic containing a first base sequential element to be clocked by a first circuit clock and a second base sequential element to be clocked by a second circuit clock, said FPD comprises:

a first modified sequential element to receive a global clock and said first circuit clock, said first modified sequential element containing said first base sequential element, said global clock being connected to a clock input of said first base sequential element, said first base sequential element transitioning to a next state only after occurrence of a transition on said first circuit clock and transition to said next state being timed according to said global clock; and

a second modified sequential element to receive said global clock and said second circuit clock, said second modified sequential element containing said second base sequential element, said global clock being connected to a clock input of said second base sequential element, said second base sequential element transitioning to a next state only after occurrence of a transition on said second circuit clock and transition to said next state be-

ing timed according to said global clock.

[c2] 2. The FPD of claim 1, wherein timing the transitions of said first base sequential element and said second base sequential element according to said global clock avoids problems due to any substantial skew present between said first circuit clock and said second circuit clock.

[c3] 3. The FPD of claim 2, wherein the clock period of said global clock is more than the maximum skew between said first circuit clock and said second circuit clock.

[c4] 4. The FPD of claim 2, wherein said FPD is used to validate a logic design of said circuit logic.

[c5] 5. The FPD of claim 1, wherein said first modified sequential element further comprises:
a first multiplexor selecting an output of said first base sequential element if a select input to said first multiplexor is at a first logic level, and selecting a data input if said select input is at a second logic level, wherein said data input is designed to be an input to said first base sequential element according to said circuit logic, said multiplexor providing said output as an input to said first base sequential element; and
a detect block generating said select input such that said select input changes from said first logic level to said

second logic level after occurrence of a transition on said first circuit clock.

[c6] 6. The FPD of claim 5, wherein said detect block is shared by said first modified sequential element and said second modified sequential element.

[c7] 7. The FPD of claim 1, wherein said FPD comprises a FPGA.

[c8] 8. An apparatus implementing a circuit logic in a field programmable device (FPD), said circuit logic containing a first base sequential element to be clocked by a first circuit clock and a second base sequential element to be clocked by a second circuit clock, said apparatus comprising:

means for transitioning said first base sequential element to a next state after the occurrence of a transition on said first circuit clock, transition to said next state of said first base sequential element being timed according to a global clock; and

means for transitioning said second base sequential element to a next state after the occurrence of a transition on said second circuit clock, transition to said next state of said second base sequential element being timed according to said global clock.

[c9] 9. A method of implementing a circuit logic in a field programmable device (FPD), said circuit logic containing a first base sequential element to be clocked by a first circuit clock and a second base sequential element to be clocked by a second circuit clock, said method comprising:

transitioning said first base sequential element to a next state only after the occurrence of a transition on said first circuit clock, transition to said next state of said first base sequential element being timed according to a global clock; and

transitioning said second base sequential element to a next state only after the occurrence of a transition on said second circuit clock, transition to said next state of said second base sequential element being timed according to said global clock.